**IN THE CLAIMS**

*Please amend the claims as follows:*

1-11 (Cancelled)

12. (Currently Amended) A PLL frequency synthesizer comprising:

a voltage control oscillator [[of]] for changing an oscillation frequency, depending on a potential of an oscillation frequency control signal;

a frequency divider [[of]] for dividing an output signal from the voltage control oscillator with a predetermined frequency division ratio;

a phase comparator [[of]] for receiving an output signal from the frequency divider and an external reference signal, detecting a difference in phase between the output signal and the reference signal, and outputting a phase difference signal;

a charge pump circuit [[of]] for causing a constant current to flow in or out, depending on the phase difference signal from the phase comparator;

a loop filter [[of]] for filtering out a high frequency component of an output of the charge pump circuit, converting the current flowing into or out of the charge pump circuit into a voltage, and outputting the voltage as the oscillation frequency control signal; and

a linearization circuit [[of]] for controlling a gain of the charge pump circuit so as to compensate for nonlinearity of a loop gain of the PLL frequency synthesizer with respect to the oscillation frequency control signal,

wherein the linearization circuit has a plurality of transistors [[of]] for receiving the oscillation frequency control signal from the loop filter and changing flowing currents, depending on a potential of the oscillation frequency control signal, and

the gain of the charge pump circuit is continuously controlled, depending on a sum of the currents flowing through the plurality of transistors.

13. (Previously Presented) The PLL frequency synthesizer of claim 12, wherein the plurality of transistors of the linearization circuit have different threshold voltages from each other.

14. (Currently Amended) A PLL frequency synthesizer comprising:

a voltage control oscillator [[of]] for changing an oscillation frequency, depending on a potential of an oscillation frequency control signal;

a frequency divider [[of]] for dividing an output signal from the voltage control oscillator with a predetermined frequency division ratio;

a phase comparator [[of]] for receiving an output signal from the frequency divider and an external reference signal, detecting a difference in phase between the output signal and the reference signal, and outputting a phase difference signal;

a charge pump circuit [[of]] for causing a constant current to flow in or out, depending on the phase difference signal from the phase comparator;

a loop filter [[of]] for filtering out a high frequency component of an output of the charge pump circuit, converting the current flowing into or out of the charge pump circuit into a voltage, and outputting the voltage as the oscillation frequency control signal; and

a linearization circuit [[of]] for controlling a gain of the charge pump circuit so as to compensate for nonlinearity of a loop gain of the PLL frequency synthesizer with respect to the oscillation frequency control signal,

wherein the linearization circuit has a transistor [[of]] for receiving the oscillation frequency control signal from the loop filter and changing a flowing current, depending on a potential of the oscillation frequency control signal,

the linearization circuit has a bias voltage generating circuit [[of]] for generating a bias voltage,

a source voltage of the transistor of the linearization circuit is controlled to be the bias voltage of the bias voltage generating circuit ~~is input to a source of the transistor of the linearization circuit~~, and the oscillation frequency control signal from the loop filter is input to a gate of the transistor of the linearization circuit, and

the gain of the charge pump circuit is continuously controlled, depending on a value of the current flowing through the transistor.

15. (Previously Presented) The PLL frequency synthesizer of claim 14, wherein the transistor of the linearization circuit is composed of a plurality of transistors, and

the gain of the charge pump circuit is continuously controlled, depending on a sum of currents flowing through the plurality of transistors.

16. (Previously Presented) The PLL frequency synthesizer of claim 15, wherein the bias voltage generating circuit generates a plurality of different bias voltages, and

the different bias voltages from the bias voltage generating circuit are input to respective sources of the plurality of transistors of the linearization circuit.

17. (Previously Presented) The PLL frequency synthesizer of claim 16, wherein the bias voltage generating circuit changes the plurality of generated bias voltages based on an externally input bias voltage setting signal.